Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently amended) A method for communication between an IC (integrated circuit) and an external RAM (random access memory), where the external RAM has at least one memory bank and communication between the IC and the external RAM is performed via two or more channels, a channel is defined by its physical characteristics regarding at least throughput and latency, where data exchange between the IC and the external RAM necessitates at least two memory bank commands, the method comprising:

transmitting the at least two memory bank commands via multiple channels;

prioritizing the at least two transmitted memory bank commands on the basis of a static priority allocation; and

further prioritizing the at least two commands having the same static priority on the basis of a dynamic priority allocation for the channels.

2. (Previously presented) The method according to Claim 1, wherein the prioritizing the at least two transmitted memory bank commands on the basis of a static priority allocation includes:

giving a 'Burst Terminate' command the highest priority,

giving a 'Read' or 'Write' command the second highest priority,

giving an 'Activate' command the third highest priority, and

giving a 'Precharge' command the lowest priority.

3. (Previously presented) The method according to Claim 1, wherein the prioritizing the at least two commands having the same static priority on the basis of a dynamic priority allocation for the channels includes:

giving the lowest priority to a channel via which a command has been sent.

4. (Previously presented) The method according to Claim 1, wherein the prioritizing the at least two commands having the same static priority on the basis of a dynamic priority allocation for the channels includes:

giving one of the channels the highest priority in the next clock cycle if this channel does not have the highest priority in the current clock cycle and a command is sent via another channel.

5. (Previously presented) The method according to Claim 1, wherein the prioritizing the at least two commands having the same static priority on the basis of a dynamic priority allocation for the channels includes:

withdrawing the highest priority of a channel only when this channel can send a command.

6. (Previously presented) The method according to Claim 1, wherein the method further includes accessing physically separate memory areas in the external RAM via the channels.

7. (Previously presented) The method according to Claim 1, wherein the method further includes accessing jointly used memory areas in the external RAM via the channels and the assurance is given that no successive access operations to a jointly used memory area will arise.

8. (Previously presented) The method according to Claim 1, wherein the method further includes accessing various memory banks via at least one channel by a network.

9. (Previously presented) The method according to Claim 1, wherein the method further includes always having an access operation to another memory bank effected between two access operations to a memory bank.

10. (Previously presented) The method according to Claim 1, wherein the method further includes permitting two successive access operations to a memory bank when the access operations are made to the same row in the memory bank.

11. (Previously presented) The method according to Claim 1, wherein the method further includes depicting the states of the memory banks by associated state machines.

12. (Previously presented) The method according to Claim 1, wherein the method further includes using a plurality of RAM modules and transmitting a chip enable signal in order to select the desired module.

13. (Currently amended) A memory controller for an IC (integrated circuit) with an external RAM (random access memory), where the external RAM has at least one memory bank and communication between the IC and the external RAM is performed via two or more channels, a channel is defined by its physical characteristics regarding at least throughput and latency, where data exchange between the IC and the external RAM necessitates at least two memory bank commands, the memory controller comprising:

a command scheduler which prioritizes transmissions of the at least two memory bank commands of multiple channels on the basis of a static priority allocation for commands and the commands having the same priority are further prioritized by the command scheduler on the basis of a dynamic priority allocation for the channels.

14. (Previously presented) An appliance for reading and/or writing to storage media, wherein the appliance comprising a memory controller utilizing the method according to Claim 1.